Chapter 16. Control System

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16.1. Overall Architecture of Fermilab Controls

The overall architecture of Fermilab control systems follows the standard design shown in Figure 16.1. Individual Front End Computers that control accelerator hardware are networked to each other, to console computers, and to various Servers using a Local Area Network. The network connections contain 10 MHz, 100 MHz, and 1 GHz Ethernet segments and switches and routers as needed, so that Control Room Consoles may access data for all the accelerators. Fermilab device naming convention is a single letter that designates the machine where the device is located, a colon, and a 6-character device name. Accordingly, Proton Driver devices will be of the form **P:devnam**, where the P: indicates that devices reside in the Proton Driver.

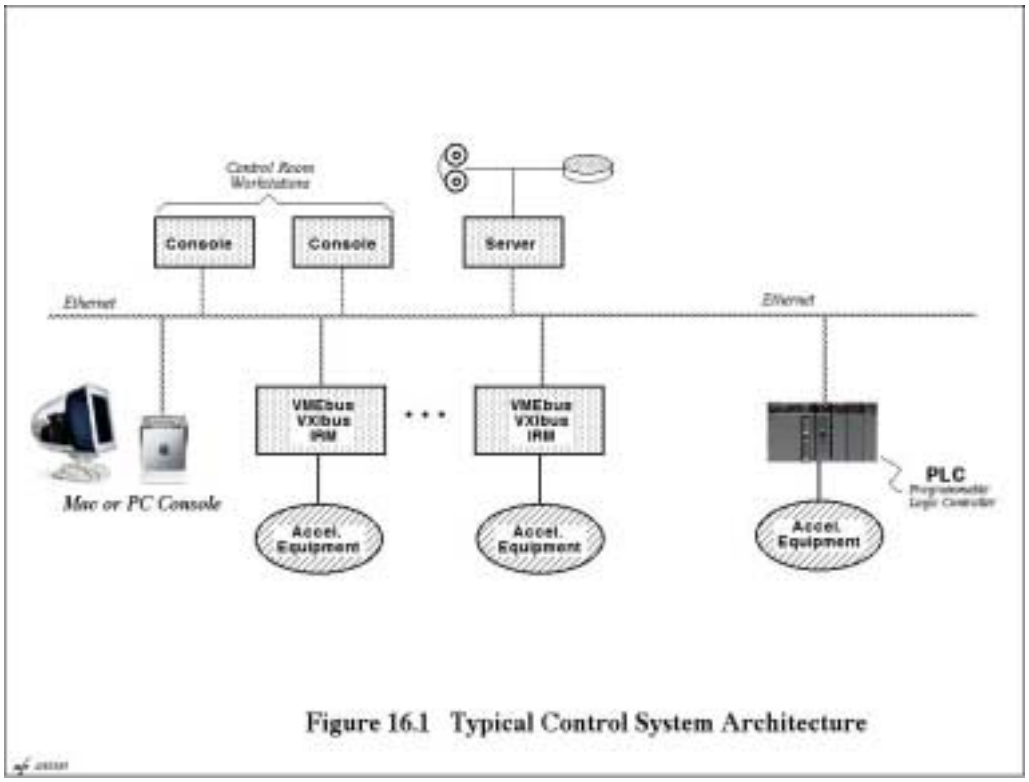

Figure 16.1 Typical Control System Architecture

To the Fermilab Control System, the Proton Driver must appear as one more accelerator in the complex. It will be operated from the Main Control Room, and data from the Proton Driver will be presented on console displays along with data from other Fermilab accelerators. Therefore, the Control System for the Proton Driver will be very similar to control systems for other machines and will use much of the same hardware and software. Although control system hardware changes rapidly, the description in this report assumes that the Proton Driver control system will be built using today's technology and products.

16.1.1. Compatibility with existing Controls

The Proton Driver controls will be organized in the same way as control systems for the other Fermilab accelerators. Parameter information will be stored in the central database, displays will be handled by the same console computers, Front End computers will connect to the accelerator hardware and requested data from the Front End computers will be sent to the console computers as needed.

16.1.2. 15 Hz Considerations

The Proton Driver is a 15 Hz machine, and data acquisition must operate synchronously at that repetition rate. Because the existing Linac control system Front End computers operate synchronously at 15 Hz, that design will be used throughout the Proton Driver. Each 15^{th} of a second, analog and digital data is read from the hardware by the Front End and made available to remote requestors. Analog data is scanned to find readings that are in alarm, that is, readings that differ from the nominal value by more than a selected tolerance. Similarly, digital readings that are not in the nominal state are considered to be in alarm. Parameters that are newly in alarm are reported to the central computers each cycle. Each parameter can be set to cause a Beam Inhibit when it is found to be in alarm.

The beam inhibit function will be useful to limit the amount of beam loss during commissioning and later in operation. When a beam inhibit occurs, it will be latched for a time that can be set by the operator. This will allow the operator to shorten the inhibit time when the machine is operating at lower current levels or at the reduced repetition rates often used during commissioning.

16.1.3. Front End Computers

The Front End computers are based on a Motorola VMEbus-based single board computer, MVME2400. VxWorks is used as the real-time operating system, the operating system that is the Fermilab standard for Front End computers. Linac Front End computers include all the software needed to control a 15 Hz machine. Each cycle, the signals from equipment attached to the system are read and stored in a local database. Remote computers may request data from the Front End computers to be returned at selected intervals up to and including 15 Hz. Because the data are read once per cycle and kept in a local database, multiple remote hosts that request the same data get exactly the same values. The local database for each Front End includes the name of the channel and the data necessary to convert the raw reading into engineering units. Also, each channel may be monitored, in which case the nominal value and tolerance are also stored locally. Fixed data, including the most recent settings, are stored in the non-volatile memory. At power-on time, the local station knows the most recent settings and can restore these settings, both analog and digital, to the hardware.

Each Front End controls different equipment and typically has different tasks to perform, such as closed loop regulation of special devices. To accommodate these

differences, Front Ends allow for small, separately compiled programs, called Local Applications, to be downloaded and stored in the non-volatile RAM. These programs can be triggered to run each 15^{th} of a second. Such programs are used in the Linac to regulate rf gradients and to control the gas flow in the ion source.

16.1.4. Network

Ethernet is the network used for all Fermilab accelerators. Each VMEbus CPU card includes a 10/100 MHz Ethernet port. Category 5 cabling will connect each CPU to a separate port on a local Ethernet switch. The uplink from individual switches will be concentrated in another 100 MHz switch that has a 1 GHz uplink connection that will connect to a router in the Computer room by way of a single-mode fiber.

16.2. Data Acquisition Hardware

Wherever possible, the Proton Driver will use some of the same data acquisition hardware used in other Fermilab accelerators. A variety of hardware exists and can be replicated as needed for various parts of the Proton Driver.

16.2.1. Internet Rack monitor

For many locations an Internet Rack Monitor, IRM, will be used. This device includes a short VMEbus card cage, the MVME2400 CPU card, a 64 channel A-D, 8 D-A outputs, and eight bytes of digital I/O, all contained in a 3U chassis. This forms a stand alone Front End that attaches to the network using the Ethernet port provided on the CPU card. Additional digitizers, D-As, and VMEbus cards may be added as needed.

16.2.2 Hot-link Rack Monitor, HRM

A recently developed digitizer system allows for 64 analog inputs, each sampled and digitized at a 10 kHz rate. The HRM is a self-powered remote chassis that connects to a PMC receiver card in a VME bus Front End computer. Communication between the PMC card and the HRM chassis uses a high-speed serial connection, Hot-link, with a serial bit rate that can be selected as 160 or 320 MHz. Individual HRM registers, such as digital I/O and D-A registers appear as PCI memory locations to the VME bus host computer. The analog subsystem autonomously reads all 64 channels at 100 μs intervals, and sends the results to the PMC interface card, where analog data is stored in a circular buffer memory. Two megabytes of RAM are used for the buffer, enough to hold 16K sets of readings for all 64 channels. Old data is overwritten by new data after 1.6 seconds. Remote hosts may request data about any group of channels to make fast time plots at sample rates of 10 kHz or slower. This is fast enough to examine power supplies for ripple and to examine the envelope of rf and beam related parameters during the 38 ms acceleration cycle, for example.

The HRM can also accommodate one daughter board designed for some special purpose. An example daughter board is an 8-channel quick digitizer that can record signals at digitizing rates up to 10 MHz. These can be used to make snapshot recordings of signals such as BPM and Beam Toroids in the transport lines and Linac related signals. Up to 16k samples per channel are recorded. The digitize trigger can be set at regular intervals or can be provided externally to synchronize the digitizer to external events such as the beam revolution period. The HRM system also includes 8 analog D-A output signals that can be used as analog reference voltages for power supplies. Additional analog outputs can be provided by installing commercially available modules in VME bus crates. VME bus cards, Industry Pack or PMC mezzanine modules are typically used for this purpose.

16.2.3. Digital I/O

Eight bytes of digital I/O are included in each digitizer system. These can be configured by the byte as either input or output and used for digital control outputs and digital status inputs. As with the analog output signals, mezzanine modules or VMEbus cards may be used to expand the amount of digital I/O.

16.2.4. Programmable Logic Controllers

Programmable Logic Controllers, PLCs, provide a cost-effective method for interfacing to some types of external hardware. These devices have been used at Fermilab to control equipment such as power supplies and ion sources. A variety of commercial analog and digital interface modules are available. The PLCs are nodes on the control system Ethernet network and can be programmed and monitored over the network.

PLCs are particularly useful for controlling stand-alone systems and high availability systems that are best configured to be independent of the control system's Front End computer. Programming of the PLCs can often be done by the group that is responsible for a given system. Simple shared-memory protocol between the PLC and the Controls Front End computer allows control and monitoring of the PLC-based systems by storing settings and reading values within the PLC's memory space.

16.2.5. Power Supply Controls

It is assumed that the power supply - controls interface is the same as the Fermilab standard that provides for ON-OFF-RESET commands using isolated relay contacts, one byte of digital status readback, analog readback signals for both power supply current and voltage, and an analog input. For a programmable power supply, an appropriate waveform would be provided to the analog command input. For power supplies that require 15 Hz waveforms, the program voltage will be generated from a 1-2k word memory that is sequentially output through a digital to analog converter. Calculation of the waveform data will be done in an upper level computer and downloaded to the Front End computers as needed. The waveform generators will be packaged with 8 channels

contained on a single VME bus board. Multiple Waveform Generator boards will be installed in Front End computers.

Digital control of the power supplies requires commands for ON, OFF, and RESET using momentary relay contact closures or openings. A 2-byte digital I/O connector from an IRM or an HRM will connect to a power supply interface fanout chassis. This chassis can accommodate 16 power supplies. Two such chassis can be attached to an IRM, the limit being the 64 analog channels available.

16.2.6. Event Clock, TCLK

Event timing for accelerators is distributed within the Fermilab complex using TCLK, a system that has 8-bit events encoded on a 10 MHz pulse train. Fanout chassis provide clock signals to equipment where timing information is needed, and the clock signal is decoded internally in equipment using programmable gate array logic. Most pulsed devices can be triggered by pulses programmed to appear at a time that is set as a delay following a selectable event. The minimum time resolution is 100 nanoseconds.

16.2.7. Beam Sync Clock

In addition to the event timers that use TCLK, there is a need for a Beam Sync clock. This clock will be generated by the Low Level RF system, and it would be used by the beam instrumentation systems to trigger the digitizer cycles to acquire turn-by-turn data from the circulating beam.

16.3. Linac Controls

Modifications to the Linac will require a modest increase in the Linac control system to accommodate the new ion source, the RFQ, and the associated beam instrumentation. This part of the project resembles the PET project that was done at Fermilab a few years ago. One IRM will be located at Ion Source potential, connected to the ground based Ethernet switch using a fiber optic Ethernet link. Other IRMs will be used for the RFQ, the LEBT, RF systems, instrumentation, and the first drift tube Linac tank. Details of the Controls and beam instrumentation for the Linac improvement can be found in Chapter 13, Section 13.8.

16.4. Controls for the 400 MeV Transport Line

Controls for the 400 MeV line include the control and monitoring of the beamline power supplies have not yet been done. Data acquisition from the beam instrumentation is listed in Chapter 15.

16.5. Synchrotron Controls

16.5.1 Ring Magnet Power Supply

Control of the ring magnet power supply will be similar to the technique used in the Main Injector. An embedded processor will try to match the requested field using the measured transfer functions, and a learning mode will help improve the accuracy. This system will be structured as a controls coprocessor inserted in the VMEbus crate containing the magnet regulator system. Using shared memory communication, the Controls processor will provide the ring magnet controller with the requested amplitude and phase of the 15 Hz and the 30 Hz components of the field.

16.5.2. Correction Element Controls

Each correction element will be driven by an analog waveform that is input to each correction element power supply. A multi-channel waveform generator will be designed for this purpose. It will be a VMEbus card that controls eight correction elements. Each channel will have a 1 k word buffer that will be played out each 15 Hz cycle. The digital waveform can be modified from the control room and downloaded to the appropriate correction element.

16.5.3. Sextupole correction

Control of the sextupole magnets will be the same as that used for other correction elements in the ring. There are 2 sextupole current busses each powered by a separate programmable power supply.

16.6. RF Controls

16.6.1. Low Level RF

The Low Level RF system, LLRF, will be configured as a VXI crate that contains its own processor board. Connection to the control system will be made using an additional Controls processor board, mounted in the VXI crate, that has shared-memory access to the Low Level settings and readings. The Controls processor functions as a normal Front End to provide communication with the central control system. LLRF data read by the Controls processor and settings sent to the Low Level system will appear the same as communications with any other Front End. The addition of the Controls processor completely separates the control system functions from the Low Level functions performed by the LLRF processor. This technique has been used in the klystron area of the existing Linac.

16.6.2. High Level RF

The control system connection to the High Level rf systems, HLRF, will be made using an Internet Rack Monitor. This type of interface is used in the existing Booster HLRF systems. For Stage 1, much of the Booster HLRF systems can be reused.

16.7. Water System Controls

The LCW system will be controlled by PLCs as needed. These PLCs will be connected to Ethernet. A Front End computer will control their operation. This configuration isolates the water system from power interruptions to its Front End computer.

16.8. Vacuum Controls

Vacuum controls for the Proton Driver will be the same as those used in other accelerators at Fermilab. Although these vacuum systems use proprietary hardware, both hardware and software exist and can be replicated for the Proton Driver. The hardware consists of a card cage, called a CIA crate that connects to the Front End using Arcnet. Existing cards for this system include digitizers to read parameters such as ion pump currents, Pirani gauges, and ion gauges, and cards that handle the logic to control the opening of sector valves. The Front End software for this system also exists.

16.9. Diagnostics Interface

Signals from beam instruments will be processed to present signal levels on the order of a few volts so the standard Controls A-Ds can be used. Signals that are slowly varying can be digitized directly; faster pulses will require sample-and-hold amplifiers. If the shape of pulsed signals is needed, A-D inputs with sampling rates up to 10 MHz are available. Very fast signals, such as wall current monitors, will need to be digitized in a fast digital oscilloscope.

16.10 Commercial Instrument Interface

16.10.1 IEEE-488

In some cases, commercial instruments need to be connected to the control system. Older instruments that use IEEE-488 will be connected using a device like the National Instruments ENET module. This device receives Ethernet messages and outputs them as IEEE-488 commands.

16.10.2 Ethernet

Recently, commercial instruments have become available that use Ethernet as the connection to external systems. If there is a choice, Ethernet is preferred over IEEE-488.

16.11 Software

Much of the existing Fermilab control system software is directly usable for the Proton Driver. The standard control room parameter pages and plotting packages can be used without modification. However, some new programs specific to the Proton Driver will be needed.

16.11.1. Front End Software

Additional local applications will be needed to perform regulation of the RFQ gradient, the ion source operating characteristics, and so forth, but most of the core functions of the Front End software will be needed and can be used without modification.

16.11.2 Console Application programs

A few new application programs will be needed to control and display information about Proton Driver systems. These include applications for the RFQ, transport line tuning, rf systems, injection and extraction.

16.12 Beam Permits, Beam Inhibit, e-Berm

Personnel safety for the Proton Driver will be overseen by the Fermilab ES&H Department. For operator aid and convenience, the control system's ability to inhibit beam will be used. This capability can help limit the amount of beam lost, particularly during the commissioning period.

16.13. R&D Program

During the R& D phase of the Proton Driver program, two VME bus cards should be developed: an 8-channel waveform generator and an 8-channel quick digitizer.

Although the IRM and the HRM support 8 channels of 10 MHz digitizers, some locations in the ring will need many more channels. If the digitizer is built as a VME bus card, many more channels can be accommodated in a single VME bus crate.

Similarly, many correction element waveforms will be needed at specific points in the ring. Given an 8-channel waveform generator card, a VME bus crate can contain all the waveform generators needed at these locations.

In addition to these, a power supply interface fanout chassis could be designed and built during the R&D phase of the project.